## Claims

What is claimed is:

1. An impedance-matched IQ network configured to provide substantially a ± 90 degree phase shift to a received quadrature phase signal relative to a received an in-phase signal, and to provide a summation of the ± 90 degree phase-shifted quadrature phase signal and the received in-phase signal, the impedance matched IQ network comprising:

a phase shift circuit having an in-phase mixer port configured to receive the in-phase signal, a quadrature-phase mixer port configured to receive the quadrature phase signal, a termination port, and an output port, the phase shift circuit configured to provide substantially a ±90 degree phase shift between the in-phase and quadrature-phase mixer ports; and

a back termination coupled to the termination port of the phase shift circuit, the back termination having an impedance value substantially equal to the characteristic impedance of the phase shift circuit at the termination port.

2. The impedance-matched IQ network of claim 1, wherein the termination port comprises either the in-phase mixer port or the quadrature-phase mixer port of the impedance-matched IQ network.

3. The impedance-matched IQ network of claim 1, wherein the phase shift circuit comprises at least one phase shifter.

4. The impedance-matched IQ network of claim 3, wherein the at least one phase shifter comprises a plurality of series-coupled pi- or T-type phase shifters.

5. The impedance-matched IQ network of claim 3, wherein the at least one phase shifter comprises a plurality of series-coupled distributed pi- or T-type phase shifters.

6. The impedance-matched IQ network of claim 3, wherein the at least one phase shifter comprises a plurality of series-coupled transmission line phase shifters.

7. The impedance-matched IQ network of claim 1, further comprising a matching network coupled to the output port.

8. The impedance-matched IQ network of claim 1, wherein the back termination comprises a resistive element.

9. The impedance-matched IQ network of claim 4, wherein the plurality of phase shifters comprises three series coupled pi-type L-C phase shifters, comprising:

a first pi-type L-C phase shifter comprising a first shunt inductor, a second shunt inductor, and a first series capacitor coupled therebetween;

a second pi-type L-C phase shifter comprising the second shunt inductor, a third shunt inductor, and a second series capacitor coupled therebeween; and

a third pi-type L-C phase shifter comprising the third shunt inductor a fourth shunt inductor, and a fourth series capacitor coupled therebetween.

10. The impedance-matched IQ network of claim 4, wherein the plurality of phase shifters comprises three series-coupled T-type L-C phase shifters, comprising:

a first T-type L-C phase shifter comprising a first series capacitor, a second series capacitor, and a first shunt inductor coupled therebetween;

a second T-type L-C phase shifter comprising the second series capacitor, a third series capacitor, and a second shunt inductor coupled therebetween; and

a third T-type L-C phase shifter comprising the third series capacitor, a fourth series capacitor, and a third shunt inductor coupled therebetween.

11. An image rejection circuit, comprising:

an in-phase mixer;

a quadrature phase mixer; and

an impedance-matched IQ network coupled to the in-phase mixer and to the quadrature phase mixer, the impedance-matched IQ network comprising:

a phase shift circuit having an in-phase mixer port coupled to the in-phase mixer, a quadrature-phase mixer port coupled to the quadrature phase mixer, a termination port, and an output port, the phase shift circuit configured to provide substantially a ±90 degree phase shift between the in-phase and quadrature-phase ports; and

a back termination coupled to the termination port of the phase shift circuit, the back termination having an impedance value substantially equal to the characteristic impedance of the phase shift circuit at the termination port.

12. The image rejection circuit of claim 11, wherein the termination port comprises either the in-phase mixer port or the quadrature-phase mixer port of the impedance-matched IQ network.

13. The image rejection circuit of claim 11, wherein the phase shift circuit comprises at least one phase shifter.

14. The image rejection circuit of claim 13, wherein the at least one phase shifter comprises a plurality of series-coupled pi- or T-type phase shifters.

15. The image rejection circuit of claim 13, wherein the at least one phase shifter comprises a plurality of series-coupled distributed pi- or T-type phase shifters.

16. The image rejection circuit of claim 13, wherein the at least one phase shifter comprises a plurality of series-coupled transmission line phase shifters.

17. The image rejection circuit of claim 11, further comprising a matching network coupled to the output port.

18. The image rejection circuit of claim 11, wherein the back termination comprises a resistive element.

19. The image rejection circuit of claim 14, wherein the plurality of phase shifters comprises three series coupled pi-type L-C phase shifters, comprising:

a first pi-type L-C phase shifter comprising a first shunt inductor, a second shunt inductor, and a first series capacitor coupled therebetween;

a second pi-type L-C phase shifter comprising the second shunt inductor, a third shunt inductor, and a second series capacitor coupled therebeween; and

a third pi-type L-C phase shifter comprising the third shunt inductor a fourth shunt inductor, and a fourth series capacitor coupled therebetween.

20. The image rejection circuit of claim 14, wherein the plurality of phase shifters comprises three series-coupled T-type L-C phase shifters, comprising:

a first T-type L-C phase shifter comprising a first series capacitor, a second series capacitor, and a first shunt inductor coupled therebetween;

a second T-type L-C phase shifter comprising the second series capacitor, a third series capacitor, and a second shunt inductor coupled therebetween; and

a third T-type L-C phase shifter comprising the third series capacitor, a fourth series capacitor, and a third shunt inductor coupled therebetween.

21. The image rejection circuit of claim 11, further comprising a first bypass capacitor coupled to the in-phase mixer, and a second bypass capacitor coupled to the quadrature-phase mixer.

22. The image rejection circuit of claim 11, wherein the in-phase and quadrature-phase mixers each comprise differential mixer ports coupled to the impedance-matched IQ network, the impedance-matched network further comprising bypass capacitors coupled to each of the in-phase and quadrature-phase differential mixer ports.

23. An impedance-matched IQ network configured to provide substantially a ± 90 degree phase shift to a received quadrature phase signal relative to a received an in-phase signal, and to provide a summation of the ± 90 degree phase-shifted quadrature phase signal and the received in-phase signal, the impedance matched IQ network comprising:

phase shifting means having an in-phase mixer port configured to receive the in-phase signal, a quadrature-phase mixer port configured to receive the quadrature phase signal, a termination port, and an output port, the phase shift circuit configured to provide substantially a ±90 degree phase shift between the in-phase and quadrature-phase mixer ports; and

termination means coupled to the termination port of the phase shifting means, the termination means having an impedance value substantially equal to the characteristic impedance of the phase shift means at the termination port.